(9) CLAIMS

1. A cellular metal-oxide-semiconductor structure having a plurality of individual field effect transistors, the structure comprising:

a poly-silicon gate construction having a predetermined geometric mesh configuration; and

subjacent each intersection of said mesh, a substantially insulative material plug inter-spaced between adjacent source regions and adjacent drain regions of said structure.

2. The structure as set forth in claim 1 wherein each said plug is fabricated of a material for reducing capacitance between said gate structure and said source regions and said drain regions of said structure.

3. The structure as set forth in claim 1 wherein each said plug has a predetermined geometric shape and dimensions associated with gate length of each of said transistors.

4. The structure as set forth in claim 1 comprising:

each said plug is a field oxide region having a thickness greater than gate oxide thickness for said transistors and extending from said gate structure into a substrate region so inter-spaced between adjacent source regions and adjacent drain of said structure.

5. The structure as set forth in claim 1 comprising:

each said plug is an insulative poly-silicon material layered in the field isolation layer

between said gate structure and a surface of said structure containing source regions and drain regions therein.

6. The structure as set forth in claim 1 comprising:

each said plug is a filled shallow trench isolation region extending into a surface of the structure containing source regions and drain regions therein.

7. A MOSFET array comprising:

a semiconductor material having a top surface;

a plurality of lateral metal-oxide-semiconductor transistors in a cellular array configuration with respect to said top surface, each of said transistors including a first region of a geometric gate construction overlying and insulated from the top surface proximate a transistor channel region between a transistor source region and transistor drain region in said top surface, said gate construction forming a mesh having a plurality of substantially identical openings, each of said opening approximating a predetermined geometric shape; and

subjacent each intersection of said mesh, each intersection forming a second region of the geometric gate construction overlying and insulated from the top surface proximate a third region of said top surface intervening adjacent source regions and adjacent drain regions of said transistors, an inherent capacitance-reducing plug.

8. The array as set forth in claim 7 wherein said capacitance-reducing plug is a volume of oxide.

9. The array as set forth in claim 8, wherein said volume of oxide has a geometric shape and geometric dimensions substantially conformed to the geometric shape and geometric dimensions of said intersection.

10. The array as set forth in claim 8 wherein said volume of oxide extends from a bottom surface of said gate construction into a predetermined depth of said top surface associated with source region and drain region depth measured from said top surface into said semiconductor material.

11. The array as set forth in claim 8 wherein said plug is a grown field oxidation material.

12. The array as set forth in claim 7 wherein said capacitance-reducing plug is a filled shallow trench isolation region.

13. The array as set forth in claim 7 wherein said geometric gate construction is so isolated from said top surface by a gate oxide layer and said capacitance-reducing plug is a layer of capacitance-reducing material floating in said gate oxide layer superjacent said top surface.

14. The array as set forth in claim 7 wherein said geometric gate construction is a poly-silicon structure having a first doping factor and said capacitance-reducing material is a poly-silicon layer.

15. The array as set forth in claim 7 wherein said geometric gate construction is a poly-silicon structure having a first doping factor and said capacitance-reducing material is a dielectric material.

16. The array as set forth in claim 15 wherein said dielectric material is thicker greater than said geometric gate construction.

17. A method for increasing switching speed in a MOSFET array wherein said array is associated with a semiconductor surface layer and includes a geometric gate construction fabricated of poly-silicon above said surface layer, the method comprising:

locating each grid intersection of said geometric gate construction; and

subjacent each said intersection, plugging a region separating adjacent MOSFET source regions and adjacent MOSFET drain regions of the array using a plug material for reducing capacitance between the poly-silicon forming the grid and said surface layer.

18. A cellular power MOSFET integrated circuit comprising:

a semiconductor substrate having a first ion doping type;

a surface layer of said substrate;

in said surface layer, an active element well having the first ion type doping,

an array of MOSFETs including at least one row of source regions and at least one row of drain regions; superjacent said surface layer, a field isolation layer, having source and drain electrical connection vias therethrough, a poly-silicon geometric gate construction, said gate construction forming a grid having a plurality of substantially identical

openings of a predetermined geometric shape and dimensions, a gate oxide layer separating said gate construction from said surface layer; and

a capacitance-reducing plug at each intersection of said grid such that said plugs are inter-spaced between adjacent source regions of transistor source rows and adjacent drain regions of transistor drain rows of each row of the array.

19. The invention as set forth in claim 18 wherein said plug is a relative thick field oxide.

20. The invention as set forth in claim 18 wherein said plug is a dielectric floating gate construction in said gate oxide layer.

21. The invention as set forth in claim 18 wherein said plug is a trench isolation insulator.

22. The invention as set forth in claim 18 wherein said plug a construction formed of one or more of a relative thick field oxide, a polysilicon floating gate construction in said gate oxide layer, and a trench isolation material.